AMENDMENTS TO THE SPECIFICATION

Replace the paragraph on page 1, lines 15-16, with the following:

DYNAMICALLY RECONFIGURABLE UNIVERSAL TRANSMITTER SYSTEM
Ser. No. 09/922,484, filed August 3, 2001, now Patent No. 7,233,810, issued June 19, 2007

Replace the paragraph beginning on page 12, line 13, with the following:

In another embodiment, hardware resources 102B, e.g., finger elements 156a through 156n, are limited to performing a single communication protocol, while in another embodiment; hardware resources are configurable to perform any one of a wide range of communication protocols. For example, co-pending U.S. patent application Ser. No. 09/751,783, entitled "A Configurable All-Digital Coherent Demodulator System for Spread Spectrum", by Ravi Subramanian, filed December 29, 2000, now Patent No. 7,010,061, issued March 7, 2006, is configurable to accommodate a wide range of communication protocols. This related application is commonly assigned, and is hereby incorporated by reference.

Replace the paragraph beginning on page 21, line 8, with the following:

Referring now to FIG. 3D is a table of computer memory fields that track users of software-based allocation and scheduling of hardware resources, in accordance with one embodiment of the present invention. Primary table 380A lists groups of hardware resources by a group identification in column 381 and by a pointer to a secondary table that identifies the start location for the control information on the hardware resources slated for the group. Primary table can provide a reference back to an ID table, e.g., table 350. The last entry in primary table is for B, after which the fist line in primary table is resume, e.g., pointer end traverses to the first line of the table. Secondary table includes an on/off column to turn control parameters for a hardware resource either on or off. No link list is listed in column 389 for all the entries in a group, e.g., first block A 370. This is because each entry has a default pointer to the next line in the table. In this manner, total flexibility throughout the table is eliminated at the benefit of ease of implementation and speed through which the table may be traversed. However, a link address can be implemented for any line of a hardware

resource. This list can be referred to as a chunk list in that all the hardware elements in first block A 370 are implemented in a sequential fashion as the default address link sequence. While the present embodiment provides a specific quantity of table and columns in each table, the present invention is well suited to utilizing more or less columns with different types of information for other purposes. The flexibility and implementation ease of the present invention is still maintained with these alternative embodiments. Additional information on the design and implementation of primary and secondary tables 308A and 380B respectively, is provided in co-pending U.S. patent application Ser. No. 09/922,484 entitled "DYNAMICALLY RECONFIGURABLE UNIVERSAL TRANSMITTER SYSTEM" by Medlock et al., filed August 3, 2001, now Patent No. 7,233,810, issued June 19, 2007. This related application is commonly assigned, and is hereby incorporated by reference.